PRODUCTION DC SCREENING FOR RF PERFORMANCE OF A 900 MHZ MONOLITHIC LOW NOISE AMPLIFIER

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ABSTRACT

Novel approaches for production DC screening of a 900 MHz monolithic silicon bipolar low noise amplifier for noise figure and power gain are presented. The proposed techniques can be used in screening the performance of any RFIC by setting limits on the AC performance of the active devices used.

INTRODUCTION

The present commercial wireless market is extremely competitive. RFIC cost must be minimized in order to serve high volume markets, which have been dominated by low cost discrete solutions. One major element of RFIC cost is production testing. Although direct RF testing is technically feasible, it is often very expensive for low cost, high volume products.

The use of DC production testing to screen the RF performance of an RFIC is an attractive alternative to direct RF testing. DC testing capabilities are well established, and therefore the cost of adding DC screening techniques for RF performance is minimal.

In this paper we present the methods used to screen RF performance of a 900 MHz low noise amplifier (LNA) based upon measurements of DC transistor parameters. This RFIC, which contains an LNA and a mixer [1], is fabricated with Harris Semiconductor's 10 GHz f_T UHF-1 silicon based complementary bipolar SOI process [2].

LOW NOISE AMPLIFIER

Fig. 1 shows the simplified circuit schematic of the LNA, including bias network. The LNA is composed of a single common-emitter stage with a 22nH spiral inductor as a load. A single stage amplifier was sufficient to achieve the desired small signal power gain of approximately 13 dB.

To allow for low noise operation no resistive feedback or degeneration is used. The frequency dependent nature of the spiral inductor provides a low impedance at low frequencies (100 - 300 MHz) to the collector of the LNA transistor, Q1, which helps to sustain unconditionally stable operation. At RF frequencies (800 - 1000 MHz), the spiral inductor provides a high enough impedance to achieve high gain.

The bias network generates a reference voltage with the appropriate temperature coefficient to stabilize the collector current over the operating temperature range. The bias network is designed to have negligible impact on the noise figure and intercept point of the LNA, as the transistor Q1 is biased at it's base through a high value resistor, LNA_Rbias.

NOISE FIGURE SCREENING

Since the bias network and the spiral inductor contribute minimal noise, the noise figure of the LNA is dominated by the noise characteristics of the transistor, Q1. The transistor, Q1, is implemented as an NPN double base, double collector, single emitter structure.

At medium and high frequencies, the noise factor of the bipolar transistor is given by [3]

$$F = 1 + \frac{r_b}{R_S} + \frac{r_e}{2R_S} + \frac{(R_S + r_b + r_e)^2}{2\alpha_o r_e R_S}\left[\left(\frac{f}{Kf_T}\right)^2 + \frac{1}{h_{FE}}\right]$$

where r_b is the total base resistance, R_S the source resistance, r_e the emitter resistance, α_o the common-base current gain, f the frequency, f_T the cutoff frequency, and h_{FE} the common-emitter current gain. The constant K is an empirical factor, typically 1.2 for silicon.

Assuming the f_T variations are not significant, which is typically the case, and/or the frequency of operation is low enough, the term containing f_T becomes small and/or constant. Then, the noise figure of a bipolar transistor is nearly proportional to the total base resistance, at a given collector current. Therefore, by measuring the base resistance, r_b, one can infer the transistor noise figure at a given bias condition.

The base resistance of the bipolar transistor consists of intrinsic and extrinsic components: pinched and un-pinched P-base resistance, external base resistance, contact resistance, and polysilicon base resistance. Typically, the pinched P-base resistance dominates the total base resistance, and is subject to process variations in sheet resistivity as well as the lithography of the emitter. Often, the lithography and sheet resistivity variations can be as large as 50% of their nominal values. While sheet resistivity measurements are simple and routine, the variations in lithography are difficult to monitor.

In order to monitor the variations of both sheet resistivity and lithography a test structure has been developed as shown in Fig. 2. The test structure is an NPN transistor, identical to LNA Q1, except with the extrinsic P^+ base region modified to prevent the direct P^+ connection from base to base. Measurement of the resistance between the two bases allows for a relative estimate of the total base resistance (extrinsic and intrinsic), of which the intrinsic component is dependent upon the actual lithography of the emitter.

For the purpose of correlation studies, one test structure and an NPN test transistor are placed on each die of the RFIC. The test transistor was included

to accommodate wafer probing of RF performance without requiring packaged unit testing.

Fig. 3 shows the correlation between base-to-base resistance of the test structure and the 900 MHz noise figure of the test transistor. Measurement data are collected from a number of wafer lots. As can be seen in Fig. 3, excellent correlation is observed between DC base-to-base resistance and 900 MHz noise figure.

Since the test transistor is sized the same as LNA transistor Q1, with minimal emitter inductance, the noise characteristics of the LNA are nearly identical to those of the test transistor. Therefore, by setting an upper limit on the base-to-base resistance of the test structure, the noise figure of the LNA was screened to be below a specified value.

POWER GAIN SCREENING

Finding an effective screen for RF power gain, S21, was more challenging. Many DC test parameters were evaluated for correlation to RF power gain, including base resistance, beta, base to emitter voltage, and Early voltage. Of the DC parameters evaluated, the Early voltage, V_A, showed promising results.

Early voltage is an indicator of output resistance of a transistor, in addition to being a parameter that can be used to extract thermal spreading resistance of the transistor. The latter aspect of the Early voltage was used to screen for RF power gain.

The UHF-1 process uses trenches and bonded oxide SOI technology. Defects in the trenches result in high substrate capacitance, leading to low RF power gain. Due to the strong dependence of the thermal spreading resistance on the presence of the oxide isolation, as well as the geometry, transistors with trench or structural defects show abnormal thermal spreading resistance.

Therefore, the trench or structural defects can be effectively screened by measuring the thermal spreading resistance of the transistor. Thermal spreading resistance can be extracted by measuring the degradation of V_A as a function of collector current [4].

Fig. 4 shows the correlation between V_A and 900 MHz power gain of the test transistor. The transistor

is biased at a fixed base-emitter voltage where the collector current is large enough to detect the thermal degradation of Early voltage. The data group centered around $V_A=15V$ represents transistors with trench defects. Transistors with trench defects exhibit unusually low thermal spreading resistance which can be inferred by V_A closer to it's electrical-only value [5]. Therefore, a screen for high values of V_A can effectively screen for low RF power gain resulting from trench defects.

Note that in Fig. 4, the data group centered around $V_A=5V$, there is a linear correlation of power gain to V_A. It is not clear, at this point, whether this correlation is related to the thermal property of the device, or the electrical Early voltage. The physics behind this trend is under investigation.

In implementing the above results, upper and lower limits on V_A are applied to effectively screen the RF power gain of the LNA. Since the design of the LNA allows the measurement of Early voltage directly of transistor Q1, the actual V_A of the Q1 is used for production screening.

CONCLUSION

Novel techniques for DC screening of RF performance have been presented. Study results demonstrate excellent correlation between the noise figure of the bipolar transistor and the base-to-base resistance of the proposed test structure. Also, a strong correlation of thermal spreading resistance to power gain has been found.

The proposed screening techniques have been successfully implemented in the production testing of a 900 MHz monolithic LNA designed for high volume commercial applications. By measuring the base-to-base resistance of the suggested test structure, the RF noise figure of the LNA has been screened. In addition, the RF power gain has been screened by measuring the Early voltage of the LNA transistor itself at high currents.

The proposed techniques are effective in screening any RFIC by setting limits on the AC performance of the active devices used. A single test transistor can give a high level of assurance that a complex RFIC would function as intended. It is also valuable for cases in which the RFIC does not lend itself to RF wafer probing.

Typically, the variations in process parameters across a wafer are small. Therefore, the test structures are not required to be placed on every die, resulting in minimal impact to die cost.

It is true that the proposed techniques, in many cases, might not be the ultimate solution for the RF testing, especially to guarantee a small distributions in RF performance. However, these techniques can still be valuable to reduce the overall test cost by being used as a preliminary RF performance screen.

A photograph of the production RFIC die is shown in Fig. 5. The test structure and correlation transistor are located at the bottom of the die.

ACKNOLEDGEMENTS

REFERENCES

[1] S.-G. Lee, R.D.Schultz, and T.D.Brogan, "900 MHz Monolithic Low Noise Amplifier and Mixer", Conference Proceedings, RF Expo East, pp. 164-167, November 1994.

[2] C. Davis, et al, "UHF-1: A High Speed Complementary Bipolar Analog Process on SOI," BCTM 92 Digest of Technical Papers, October 1992.

[3] H. F. Cooke, "Microwave Transistors: Theory and Design," Proc. IEEE, vol. 59, pp. 1163-1181, Aug. 1971.

[4] R. M. Fox and S.-G. Lee, "Thermal Parameter Extraction for Bipolar Circuit Modeling," Electronics Letters, vol. 27, no. 19, pp. 1719-1720, Sept. 1991.

[5] R. M. Fox, S.-G. Lee, and D. T. Zweidinger, "The Effect of BJT Self-Heating on Circuit Behavior," IEEE J. Solid-State Circuits, vol. 28, no. 6, pp. 678-685, June 1993.
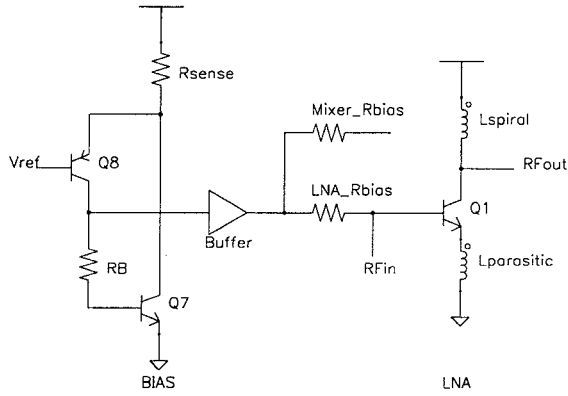
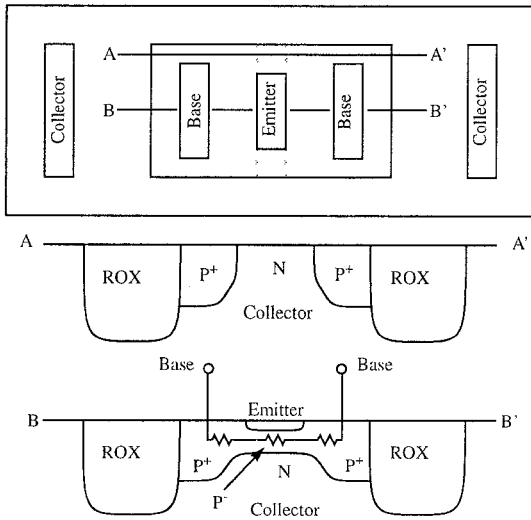Fig. 1: Simplified LNA and bias circuit schematic.

Fig. 2: Test structure for the base-to-base resistance measurement
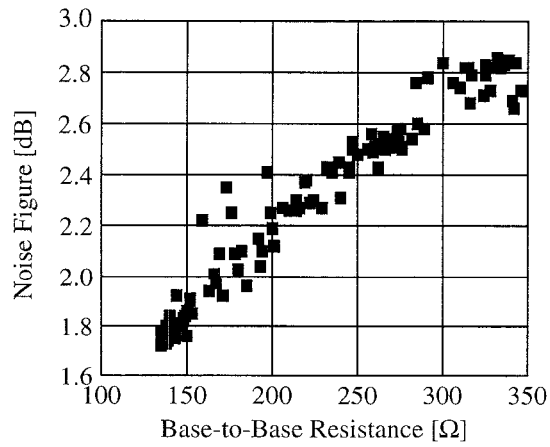

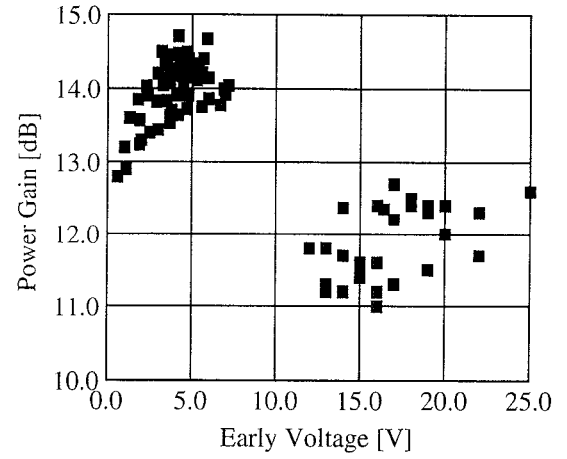Fig. 3: Plot of noise figure vs. base-to-base resistance of the test structure.
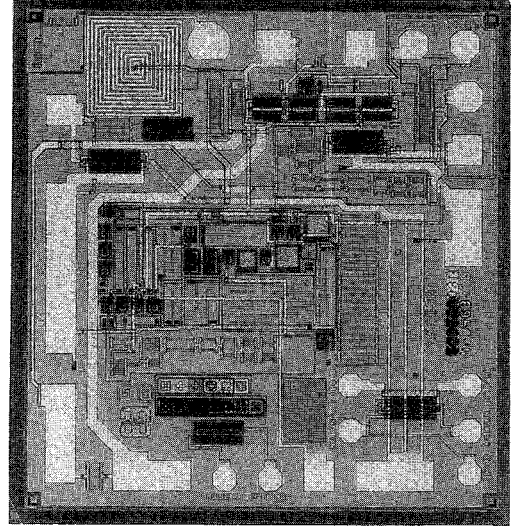

Fig. 4: Plot of the power gain vs. Early voltage.

Fig. 5: Die photograph of the RFIC (LNA/Mixer)